What is claimed is:

1. A method for charge control of a photoflash capacitor comprising the steps of:

generating an input current to induce a charge current for the photoflash capacitor when an activation signal is asserted;

detecting a first voltage from the photoflash capacitor and a second voltage corresponding to the input current;

asserting and de-asserting a recharge signal when the first detected voltage is lower and higher than a first reference voltage, respectively;

asserting and de-asserting a current limit signal when the second detected voltage is higher and lower than a second reference voltage, respectively;

asserting the activation signal only when the recharge signal is asserted and the current limit signal is de-asserted; and

providing a pin for connection of a resistive element which determines the second reference voltage.

2. The method as claimed in claim 1, wherein the input current is generated by the activation signal closing a switch to form a loop on a primary side of a transformer and cut off by the activation signal opening the switch.

3. The method as claimed in claim 1 further comprising the step of generating a constant current flowing through the resistive element, wherein the second reference

voltage is a voltage difference across the resistive element.

4. A photoflash capacitor charger operating in conjunction with a microprocessor, comprising:

a transformer generating an input current to induce a charge current for a photoflash capacitor when an activation signal is asserted;

a recharge controller detecting a first voltage from the photoflash capacitor, and asserting and de-asserting a recharge signal when the first detected voltage is lower and higher than a first reference voltage, respectively; and

a current limiter detecting a second voltage corresponding to the input current, asserting and de-asserting a current limit signal respectively when the second detected voltage is higher and lower than a second reference voltage, and asserting the activation signal only when the recharge signal is asserted and the current limit signal is de-asserted;

wherein the second reference voltage is determined by the microprocessor.

5. The photoflash capacitor charger as claimed in claim 4, wherein the current limiter comprises:

a comparator circuit asserting and de-asserting the current limit signal respectively when the detected voltage is higher and lower than the reference voltage; and

an SR latch asserting the activation signal if the recharge signal is asserted and the current limit signal is de-asserted, otherwise, de-asserting the activation signal.

6. The photoflash capacitor charger as claimed in claim 5, wherein the comparator circuit comprises:

a current source;

a resistive element having a first end coupled to the current source and a second end coupled to a ground; and

a comparator having a positive input coupled to the first end of the resistive element and a negative input receiving the second detected voltage, and outputting the current limit signal;

wherein the resistive element is adjustable.

7. The photoflash capacitor charger as claimed in claim 4 further comprising a switch coupled in a path of the input current, closed and opened respectively when the activation signal is asserted and de-asserted.

8. The photoflash capacitor charger as claimed in claim 4 further comprising a resistor coupled in a path of the input current, wherein the second detected voltage is a voltage difference across the resistor.

9. An integrated circuit for charge current limit of a photoflash capacitor, comprising:

first, second, third and fourth pins respectively for reception of a ground voltage, first detected

voltage from the photoflash capacitor and connection with a resistive element and a transformer;

a switch connected with a resistor in series between the fourth and first pin;

a recharge controller connected to the second pin for assertion and de-assertion of a recharge signal respectively when the first detected voltage is lower and higher than a first reference voltage;

a comparator circuit comprising:

a current source connected to the third pin; and

a comparator having a positive input connected to the third pin and a negative input connected where the switch and resistor is connected; and

an SR latch having a set input connected to the recharge controller for reception of the recharge signal, a reset input connected to an output of the comparator and an output connected to a control node of the switch.

10. The integrated circuit as claimed in claim 9, wherein the switch is a transistor.